Nancy Grace Roman Space Telescope coronagraph EMCCD flight camera electronics development

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ABSTRACT

The Nancy Grace Roman Space Telescope Coronagraph is a JPL-led space-based instrument that will be the most sensitive instrument ever built for direct imaging and characterization of exoplanets in the visible. The instrument contrast is expected to be better than 1e-9, which implies that it will be capable of seeing exoplanets with an apparent magnitude > 30. With such a low brightness, only a few photons per hour will be perceived by its optical detectors. Two cameras will be used on the instrument for wavefront sensing, direct imaging and spectroscopy, with frame rates ranging from 1000 fps to less than 0.01 fps. For such a broad range of operating modes and industry leading noise figure, JPL has selected the 1024x1024 CCD201-20 EMCCD from Teledyne-e2v as the image sensor for the two coronagraph cameras and appealed to Nüvü Caméras to adapt its most recent space controller design for the mission specifics. The new version of the camera readout electronics co-developed with ABB Space System group brings important improvements over the version flown at the edge of space in CSA's 2018 STRATOS campaign namely on reliability, functionality, thermal control, power, volume and mass whilst preserving its unique noise performance. This paper presents an overview of the project and addresses the development of the delivered flight modules.

Keywords: EMCCD, Nancy Grace Roman Telescope, CGI, Coronograph, Exoplanet, Photon Counting imaging, Wavefront sensing, Low light camera

1. INTRODUCTION

The Coronagraph Instrument (CGI) on the Nancy Grace Roman Space Telescope (NGRST), formerly the Wide Field InfraRed Survey Telescope (WFIRST), is a technology demonstration mission built by NASA's Jet Propulsion Laboratory (JPL). It will demonstrate the first high performance coronagraph system in space capable of visible-light exoplanet imaging of gas giants and debris disks in reflected starlight, paving the way to a future possible NASA missions aimed at imaging and characterizing fait Earth-like planets in the habitable zone,[1] such as HabEx[2] and LUVOIR.[3]

The CGI has several high-level demonstration objectives,[4] such as the autonomous ultra-precise (sub-nm) wavefront sensing and control, the use of large-format (48x48) deformable mirrors in space, high-contrast, broadband (>10% bandwidth) coronagraph masks, operation of ultra-low dark current ($\sim 10^{-4}$ e^-/pixel/s) photon counting detectors in a relevant space environment (L2 orbit), post-processing of broad-band images at unprecedented contrast levels (at least 30x better than currently demonstrated). For two of those objectives, namely the ultra-precise wavefront sensing and the low dark current photon counting detectors, JPL has selected Teledyne-e2v's Electron Multiplying CCDs (EMCCDs) as the imagers.

In the early phases of the development of the CGI, JPL had established an EMCCD test laboratory in order to advance EMCCD maturity to Technology Readiness Level (TRL) 6.[5] In the process, it was decided to baseline the commercial standard silicon CCD201-20, as opposed do the deep depletion silicon which was, and still is, of lower TRL. That maturity advancement led to the development of the CCD301, which has a few modifications to the pixel's structure to reduce the susceptibility to radiation-induced trapping sites[6,7] but remains very similar to the CCD201 with respect to the requirements of the driving electronics.

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In parallel to that work on the detectors, Nüvü Caméras has been working with the Canadian Space Agency (CSA) since the early 2010's to advance the TRL of its core technology, the EMCCD read-out electronics. The achievement of TRL-5 in 2018[8] and the flying of that technology on the balloon borne mission HiCIBaS[9] through the CSA's STRATOS program came at a propitious time. Although they were independently pursued, both achievements of the qualification of the EMCCD detector and its read-out electronics met the requirements for the CGI imaging performance. Together with the tight schedule of the Roman mission, that led JPL to contact Nüvü Caméras to procure the space-qualified read-out electronics for the CGI, which is now known as the Camera Proximity Electronics (CPE).

At that time, three cameras were envisioned for the CGI: there were plans for a dedicated Integral Field Spectrograph (IFS) channel alongside the Low Order Wavefront Sensor (LOWFS) and the Direct Imaging (DI) cameras. Although the TRL-5 milestone was reached for the read-out electronics, several key requirements of the CGI were imposing a significant design effort to be met. For instance, the initial total power budget of less than 40 W to read-out the three EMCCDs represented more than the power consumption of a single TRL-5 read-out electronics. Moreover, for each CPE the mass had to be cut by 50%, and the volume was required to shrink by about 60%. In order to accelerate the re-design and ensure meeting all of JPL's Safety Mission Assurance (SMA) requirements, Nüvü Caméras decided to team with ABB Space System to jointly design, build, and qualify the CGI CPEs.

This paper presents the main CGI requirements that had to be met by the new CPE design (Section 2), an overview of the mechanical (Section 3), thermal (Section 4), and electronic (Section 5) designs, the qualification of the flight CPEs (Section 6), and the performance with respect to the requirements (Section 7).

2. CGI REQUIREMENTS

From the initial concept involving three cameras, the CGI was descoped in the early phases of the project. With the removal of the dedicated IFS channel, there subsisted the need for only the LOWFS camera (the LoCam), and the ExCam that now serves as direct imaging and spectroscopy (Figure 1). Although the frame rate requirements between LoCam and ExCam are drastically different, it was an implied requirement that the CPEs shall be interchanged for those two cameras. In effect, both CPEs have to be identical, which means that as well as their respective primary read-out schemes, the ExCam has to implement the fast read-out of the LoCam, and the LoCam as to implement the full-frame read-out of the ExCam. Therefore, JPL provided a set of requirements that were common to both CPEs, with only a few specific requirements pertaining to the imaging (ExCam) and LOWFS (LoCam) modes. For that reason, the delivery of a single Engineering Design Unit (EDU) was planned, which covered the operational requirements of both the LoCam and ExCam. Learning from that EDU, the two final flight units could then be built and qualified. The requirements are presented in Tables 1 to 4.

Although the headboard can be seen as a simple bunch of wires connecting the CPE to the EMCCD, the high pixel rate at which the EMCCD is operated implies a very careful design of those connections. For instance, since the EMCCD horizontal clocks represent a significant capacitance ($\sim$100 pF), and since they require a swing of 10–12 Volts, it is not possible to transmit the clocking signals over a properly terminated transmission line; a serial-source terminaison would soften the clock edges beyond the required rise and fall time, and a parallel terminaison would require a very high current which would also imply a high power dissipation. Ringing between the inductance of the conductors and the capacitance of the EMCCD node are also to consider, whilst not overlooking crosstalk, the self capacitance of the transmission lines, and the carrying of the low amplitude video signal in close proximity to the fast-edged, high amplitude signals. Due to those concerns, in the early stages of the development it was decided that the Nüvü-ABB team would be responsible of the headboard that would connect the EMCCD to the CPE. Only a few high-level requirements were devised to address the thermal, mechanical, and electrical aspects of the headboard. They are summarized in Table 5.

3. MECHANICAL DESIGN

The CPEs are integrated in a 187mm x 143mm x 67mm aluminium enclosure (Figure 2). They are implemented with a two-sided folded rigid-flexible Printed Circuit Board (PCB) mounted on each side of a structural center tray (Figure 3). The digital electronics are installed on one side of the rigid-flexible PCB and the analog electronics are installed on the opposite side. The two Circuit Card Assembly (CCA) sides are connected through the flexible section of the PCB.

A framing structure and two covers are subsequently installed and result in a fully-shielded metallic enclosure (Figure 4). This enclosure is attached to the CGI optical bench with two PEEK thermally-isolating brackets.

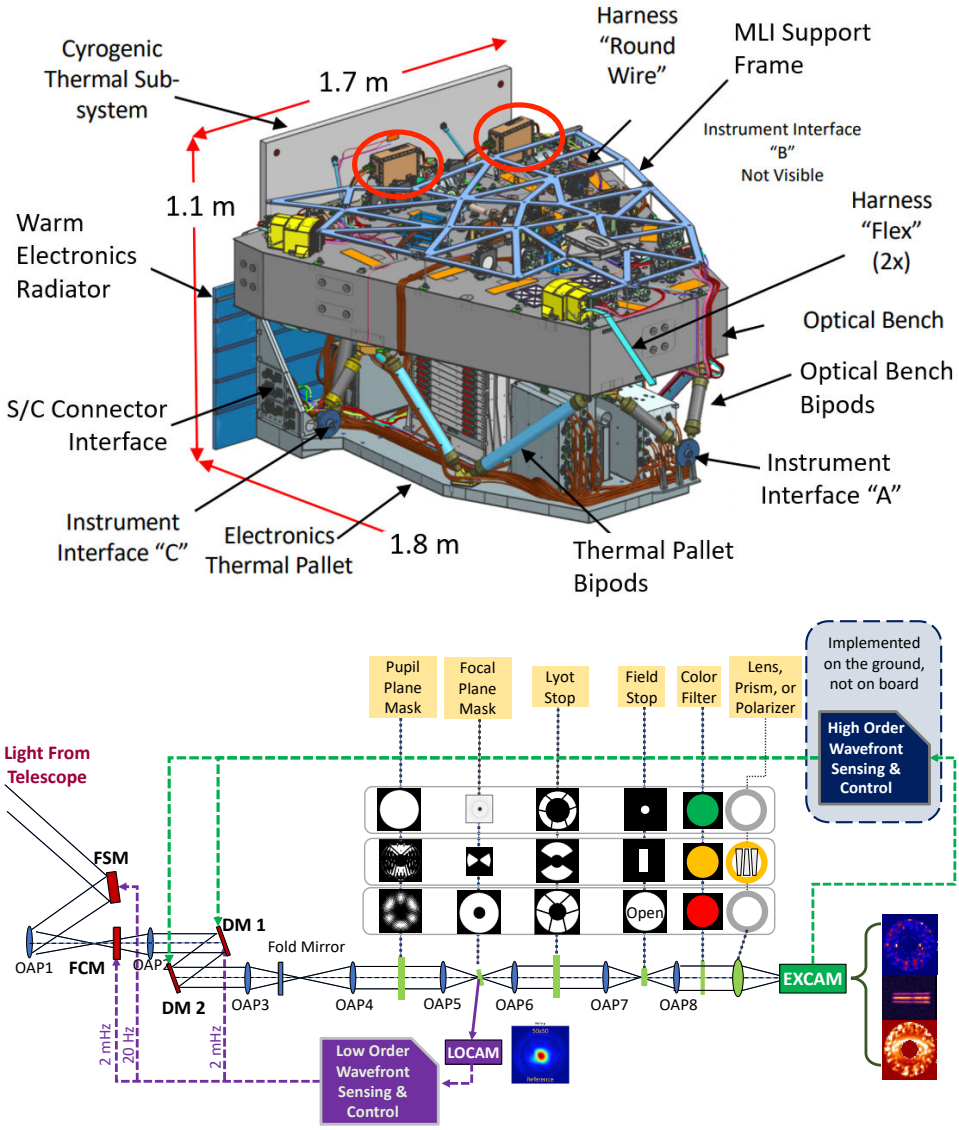

Figure 1: The CGI mechanical (**top**) and optical (**bottom**) concepts, showing the location of the LoCam and ExCam (circled in red). Figures taken from [1].

Table 1: CGI's camera electronics top level requirements

Item	Requirement		Note
Sensor	Teledyne-e2v CCD201-20		Or a flight variant
Wavelength band	450-950 nm		Dictated by sensor
Read-out modes	EM and Conventional		Adjustable EM gain from 1 to 7500x
Read-out speed	10 MHz (EM) 1 MHz (Conv)		
Read-out noise	$<$200 e^-		Real read-out noise at Photon Counting gain
Clock Induced Charges	$<$0.01 e^-/pix/frame		
Dark current	$<$2 e^-/pix/hr		
Gain stability	$<$5 %		Over 10 hours
Horizontal CTE	$>$ 0.99995		At unity gain, measured with EPER
Vertical CTE	$>$ 0.99995		Measured with EPER
Integration time	0 to 3600 s		$\leq$1 μs resolution
JPL Parts Engineering Technical Standard	Class 2 or better		
Delivery time (EDU)	12 months		From start of contract
Delivery time (Flight units)	20 months		From start of contract
	ExCam	**LoCam**	
Read-out register charge handling capacity	90 ke^-	90 ke^-	
Frame rate	0.01-1 fps	1000 fps[1]	[1]For a 50$\times$50 sub-window
Effective exposing time	Variable	$\geq$400μs[2]	[2]When running at 1k fps, external trigger
External trigger support	No	Yes[3]	[3] Trigger starts the read-out. Continuous exposure between read-out and next trigger.
Latency	–	$<$1 ms	Latency is defined as read-out time + half of the integration time

Table 2: Summary of the CGI's camera electronics environmental requirements

Item	Requirement	Note
Cooling system	Passive	Through external radiator and straps
EMCCD performance temperature	-110°C to -90°C	$\pm$0.1°C
EMCCD operating temperature	-135°C to +60°C	
EMCCD non-operating temperature	-150°C to +125°C	
Electronics operational range	-35°C to +70°C	
Electronics non-operational range	-35°C to +70°C	
CPE thermal cycling	3 cycles, -35°C to +70°C	With voltages applied
Headboard thermal cycling	3 cycles, -150°C to 65°C	Unbiased
Random vibrations	10.3 gRMS	In all axes, 2 minute/axis
First vibration mode	$\geq$300 Hz	
Thermal coupling to CGI optical bench	$\leq$0.01 W/K	
Number of environmental test units	1 EM, 2 FLT	
Vacuum environment	Yes	Design is open to vacuum
Total Ionizing Dose	10 krad	Including Reliability Design Factor of 2 (from an initial requirement of 48, which drove the pats selection)
Single Event Latchup threshold	75 Mev cm^2/mg	Or latch-up rate less than 10^{-4}/yr

Table 3: CGI's camera electronics mass, power and materials requirements

Item	Requirement	Note
Electronics mass	< 2.4 kg	Per CPE
System power	< 40 W	Sum of ExCam and LoCam
TML	$<1\%$	Total Mass Loss
CVCM	$<0.1\%$	Collected Volatile Condensable Materials

Table 4: Summary of the CGI's camera electronics requirements

Item	Requirement	Note
Pixel rate	10 MHz	
A/D bits	≥ 14	
Clock shape	Triangular	Minimizes CIC
High Voltage clock range	25–50 V	$\leq 10\%$ resolution on the gain
Sensor substrate voltage	0–7 V	≤ 0.1 V resolution
Image bias level	Adjustable	Across A/D ange
Data interface	CameraLink	Modified CameraLink, 21 bits instead of 28

The CPE enclosure first resonant mode is 304 Hz. Enclosure venting is performed through a vent fitting connected to the CGI venting interface.

The enclosure is connected to the camera head and Focal Plane Array (FPA) through a rigid-flexible headboard (Figure 5). A custom backshell is used for the headboard warm side connector and allows high-voltage clock compensation capacitors adjustment. The headboard flexible section is covered with golden tape in order to achieve low thermal emissivity.

4. THERMAL DESIGN

As they are directly installed on the CGI optical bench, the CPEs must have a minimal thermal dissipation through its mounting interface which could lead to thermoelastic distortion of the optics. The CPE PEEK thermally-isolating mounting brackets allow a thermal isolation of 0.01 W/K with respect to the CGI optical bench. CPE heat dissipation is performed through a JPL-designed thermal strap which is attached to the bottom of the CPE metallic enclosure. This thermal strap is then routed to one of the CGI passive radiators.

Each CPE enclosure thermal management scheme is designed for a worst-case dissipation of 23 W. Heat dissipated by the Xilinx Virtex-5 QV Field Programmable Gate Array (FPGA) is routed to the bottom of the CPE enclosure through a copper heatsink (Figure 7, right). On the analog CCA side, an aluminium heatsink is used to route the heat dissipated by the multiple clock power amplifiers to the metallic enclosure side (Figure 7, left). The CPE enclosure side on which the FPGA and analog amplifiers heatsink are attached is the side where the CPE thermal strap is installed.

The CPE rigid flexible PCB design also includes two thermally conductive planes which are tied to its mounting points.

Table 5: Summary of the CGI's requirements for the headboard

Item	Requirement		Note
Trace length for high speed signals	<160 mm		From the CPE's headboard connector to the mid-point of the long axis of the EMCCD
Heat conduction	0.4 mW/K		Between the CPE and the EMCCD.
	ExCam	LoCam	
Heat dissipation (EMCCD)	≤ 200 mW	≤ 1 W	Heat dissipation due to the clocking and bias voltages.

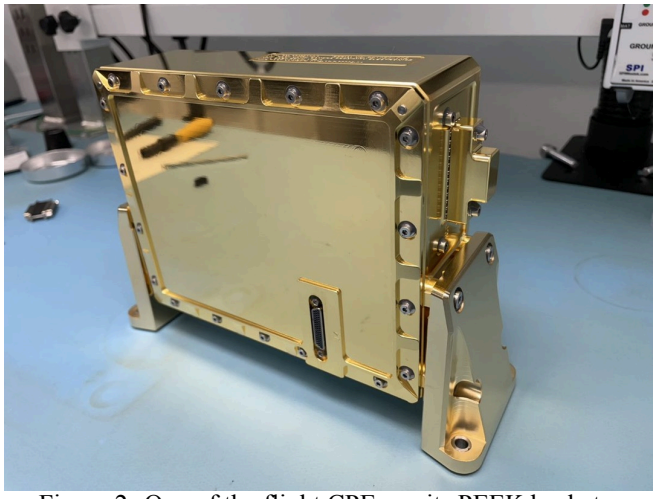

Figure 2: One of the flight CPEs on its PEEK backets.

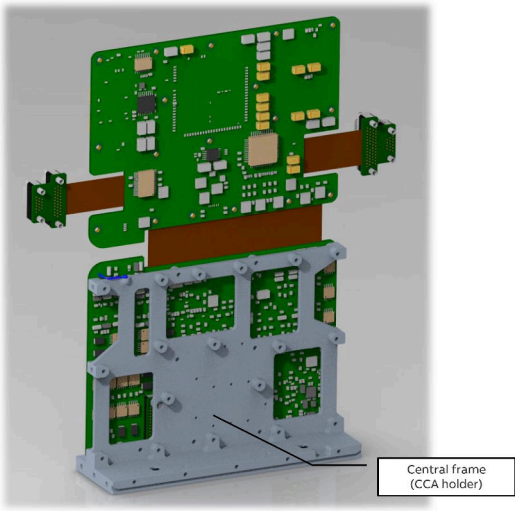

Figure 3: View of the flex-rigid PCB that composes the CPE electronics together with the center tray.

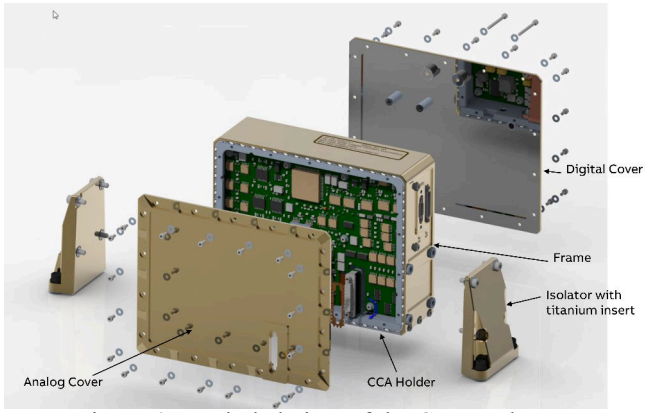

Figure 4: Exploded view of the CPE enclosure.

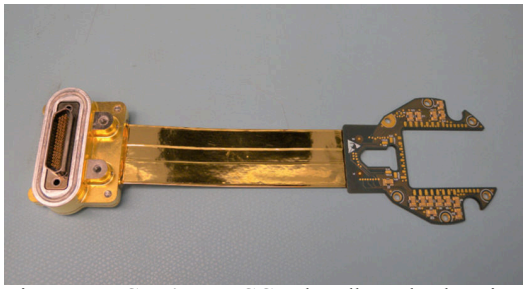

Figure 5: CPE's EMCCD headboard, showing the custom backshell and the gold tape on the flexible portion.

5. ELECTRONICS DESIGN

The electronics of the CPE can be split into two high-level components:

- The digital core, which implements the sequencer, the digital interface of the pixel data, the telemetry monitoring and the house keeping;
- The analog core, which implements the EMCCD's clocks generation and shaping, generation of DC levels, video signal conditioning and digitization.

The design of those two components were reviewed mainly under the aspects of the power dissipation, volume, and to account for JPL's SMA requirements. In order to limit the power dissipation on the optical bench and to save space, it was decided to separate the generation of the secondary voltages (-8 V, -5 V, 3.3 V, 5 V, 15 V, and 30 V), which could be placed away from the CPE, and whose responsibility went to JPL. Hence, the CPE has several inputs for those voltages, with a power-up and power-down sequences agreed on between the two teams.

It was also decided that the servo-control of the EMCCD temperature would not be handled by the CPE, once again to save space on the CGI bench. The CPE has a pass-through interface for reading two PT1000 temperature sensors that reside on the cold side of the headboard.

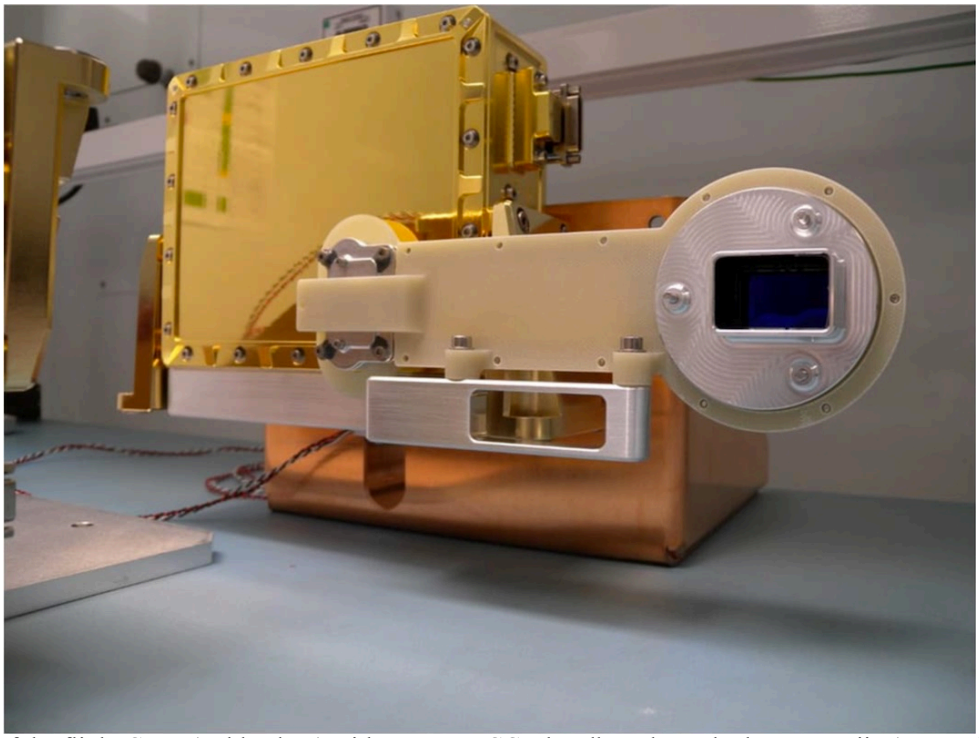

Figure 6: One of the flight CPEs (golden box) with a test EMCCD headboard attached, on a test jig (copper block) at ABB.

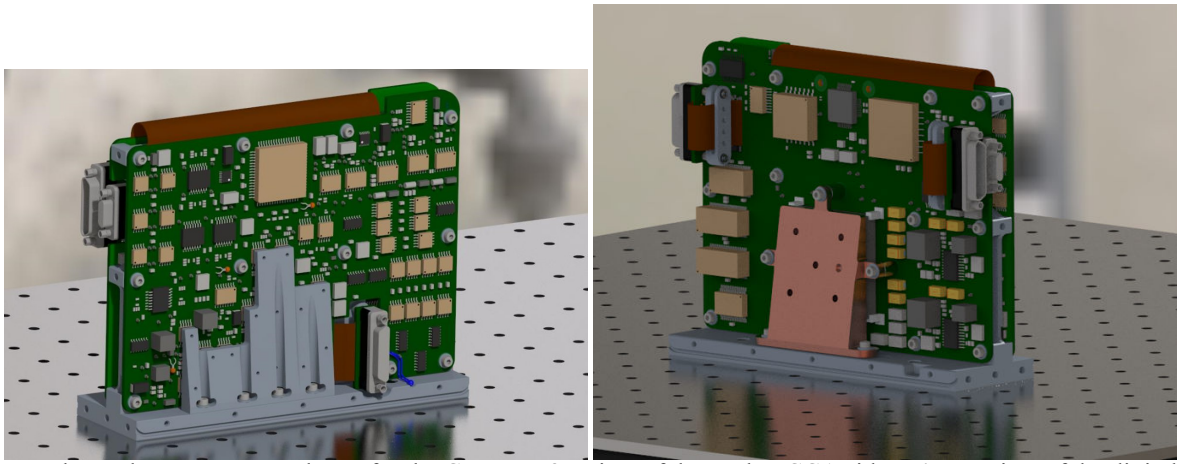

Figure 7: Thermal management scheme for the CPEs. **Left**: View of the analog CCA side. **Right**: View of the digital CCA side.

Table 6: Power dissipation of the main components of the CPE in comparison with the TRL-5 design. Numbers are for full frame read-out at maximum frame rate.

Item	TRL-5	CPE	Reduction	Note
FPGA	10–13 W	4–6 W	50–60%	Better heat dissipation on the CPE
SDRAM / SRAM	1.26 W	0.5 W	60%	SDRAM on the TRL-5, SRAM on the CPE
Clock synchronizer	0.5 W	0.5 W	0%	Same design
Low-voltage horizontal clock	1.37 W	0.47 W	64%	Per clock, 6 clocks on the TRL-5, 5 on the CPE
Low-voltage vertical clock	1.25 W	0.49 W	58%	Per clock, 8 clocks total
HV clock	0.9 W	0.5 W	45%	Same concept, optimization of quiescent power
Biases	1.18 W	0.71 W	40%	For all biases
ADC and video amplifiers	0.41 W	0.41 W	0%	Same design

5.1 Power dissipation

The drastic diminution of the power dissipation of the CPE was the requirement that drove most of the design activities. The power budget of the CGI left about a third of the power dissipation of the TRL-5 electronics[8] for each CPE to yield the same imaging performance. Fortunately, the CGI's CPEs did not had to carry the same clocking versatility as what the TRL-5 electronic implemented. With only one pixel frequency to be supported for the Photon Counting operation, major design optimizations could be made on the analog side.

It is mostly the analog clock drivers that saw a significant design change, trading versatility for lower power consumption. Although the capability to adjust individually both the high and low levels of every clock remained, the new design restricted the clock drivers to only produce a triangular shape, which was measured to be the one producing the least Clock Induced Charges (CIC).[10] By doing so, the hardware chain required to generate those clocks could be greatly simplified. Since those new clock drivers did not require the use of high speed Digital to Analog Converters (DACs), they allowed the saving of $\sim$700 mW *per clock* with that sole aspect. Another optimization involved reducing the power rails of the power amplifiers driving the clocks from $\pm$15 V to $-8/+15$V, which decreased the quiescent power by almost 25%. Also, the new clock design has the added benefit of reducing the FPGA resources used to generate them, and drastically lowered the high speed I/O count, both of which contributed to reduce the power consumption of the digital core by almost a half. Moreover, the DDR2 Synchronous Dynamic Random Access Memory (SDRAM) that was used on the TRL-5 design to allow the processing of image stacks was not necessary for the CPE and was replaced with a low power Static Random Access Memory (SRAM) of much lower capacity.

5.2 Non-volatile storage

Non-volatile memories are required to store the FPGA bit file, the embedded software image, and the definitions of the various read-out schemes.

The project required to have at least a copy of the boot files (FPGA bit file and embedded software image) in a write-protected memory, and to allow the system to be updated either during integration on the ground or in flight. It was thus decided to employ a 3D-Plus 64-Mbit Programmable Read-only Memory (PROM) as the write-protected storage, and a 3D-Plus 64-Mbit Magnetoresistive Random Access Memory (MRAM) as the updatable storage since those two are compatible with the Virtex-5's boot sequence. However, since the MRAM is known to latch-up destructively with a threshold of 8.3 Mev cm^2/mg,[11] a load switch had to be used to keep it powered off when not in use. Moreover, the load switch is configured to have a current limit of 545 mA in an attempt to mitigate the destructiveness of a latch-up, should it occur. Unfortunately, the current limit of the load switch could not be configured to the 200 mA which 3D-Plus has determined to make the latch-ups non destructive, nor could its own latch-up current limiter be employed as it is a hybrid device that would have required a Parts Engineering Technical Standard (PETS) Class 1 qualification path. Nevertheless, it was demonstrated that the likelihood of a latch-up was less than 10^{-4} per year with the intended duty cycle of the MRAM, which met JPL's requirement (Table 2).

An additional 64-Mbit NOR Flash was implemented to store the data for the read-out schemes of the cameras. That flash implements a 32-bits Cyclic Redundancy Check (CRC) every 508 bytes to check for the integrity of the data, and a redundant copy of the data to achieve a high level of robustness and availability. That flash allows the read-out schemes of the cameras to be updated during integration, and possibly in flight, should it be required.

Table 7: Static upsets in GEO for the Virtex-5. Data from [12].

Item	Value	Units	Note
SEFIs	9930	years/Device	Mean Time to SEFI
CLB-FF (filters on)	3	upsets/century	All 81920 bits
CLB-FF (filters off)	1-2	upsets/year	All 81920 bits
Configuration bits	5	upsets/year	All 34.1 million bits
BRAMs (EDAC off)	13	upsets/day	All 10.9 million bits

5.3 Digital core

The digital core mainly consists of a Virtex5-QV, the Space-grade rad-hard reconfigurable FPGA from Xilinx, built on a 65-nm copper process technology. Although newer FPGAs do exist, promising lower power consumption and higher resources density, those are mostly of the radiation-tolerant kind, with lower Total Ionizing Dose (TID) and latch-up thresholds. In the scope of this project, and in order to keep the technological and schedule risks low, it was decided to build on upon the heritage of the TRL-5 electronics, as well as Nüvü's commercial design for the digital core of the CPE. Consequently, this is what has driven the choice of the Virtex-5QV FPGA and a soft-core MicroBlaze™.

5.3.1 SEE mitigation

Several techniques are employed to mitigate the various impacts of the space radiation on the digital core of the CPE. Table 7 lists the expected static upset rates of the Virtex-5 in Geostationary Orbit (GEO), which is the closest data on hand to figure the upset rates where the NGRST will be positioned, at L2. For instance, it was decided to make sure the design operating frequency would meet the timing requirements to have the filters activated on the Configurable Logic Block (CLB) Flip-Flops (FF) (40 MHz) which virtually eradicated the need to care about Single-event Effects (SEEs) on them. Same wise, the Single-event Functional Interrupts (SEFIs) are considered to have a rate of occurence that is low enough to be neglected.

On the other hand, the Block Random Access Memories (BRAMs) exhibit an upset rate that is high enough to be considered a threat to the extended and continuous operation of the CPEs for acquisitions that can run for hundreds of hours at a time. The sequencer, which is the main VHSIC Hardware Description Language (VHDL) module that handles the realtime tasks of clocking the EMCCD and digitizing the video data, employs several of those BRAMs to store and generate the realtime data, among other things. The cache of the Microblaze is also composed of BRAMs. With an upset rate of 13 bits per day, it was decided to make use of the hardware Error Correction Code (ECC) of the Virtex-5 to detect and correct single bit errors. Those BRAMs are thus superseded by a 64-bits custom module into which the data storage is duplicated. This allows the transparent scrubbing of the redundant storage to perform Error Detection And Correction (EDAC) whilst the other is actively used, and then the storages are swapped so that the redundant becomes the active one, and the active one becomes the redundant, which allows it to be scrubbed in turn. That way, the scrubbing is completely transparent and continuous, preventing the build-up of errors that would overload the capability of the ECC to provide non-corrupted data on read operations.

Some of the hardware resources of the Virtex-5 are not protected/hardened against SEEs, such as the Digital Signal Processors (DSPs) and Phase-Locked Loops (PLLs).[13] The design of the video chain's Digital Correlated Double Sampling (DCDS) (see Section 5.5) was adapted from the commercial Nüvü Camēras design to preclude the use of the DSPs, and an external radiation tolerant clock synthesizer was used instead of the internal PLLs. Moreover, the hardware floating point unit of the Microblaze was disabled so that no DSP is used in the synthesis of the soft core processor.

For the configuration bits, the chosen approach to cope with the upsets is to detect and report them, but not to correct them. A correction would imply detecting and correcting downstream errors in the logic that could result of a momentarily wrong configuration of a CLB, which translates to managing partial device resets and error isolation, which could interrupt the image flow anyway. The detection and reporting allows for mission control to decide when it is a good time to reset the CPE to clear any error that would have accumulated, since an error is not necessarily fatal as it could affect an unused portion of the fabric. At an expected rate of 5 upsets per year, that strategy should nevertheless allow for a very limited interruption of extended acquisitions.

The Embedded Software (E-SW) is implemented in the Microblaze, which handles the house keeping, telemetry monitoring, as well as commands handling from the spacecraft. It is used to configure and supervise the real-time sequencer

Table 8: Signals generated by the CPE's analog core, measured at the headboard's end.

Signal name	Signal type	Timing resolution	Rise/fall time	Range
$S\phi_{1\text{-}4}$	Triangular clock	3.125 ns	30 V/μs	-7 V – 14 V
$I\phi_{1\text{-}4}$	Triangular clock	3.125 ns	30 V/μs	-7 V – 14 V
$R\phi_{1\text{-}3}$	RC clock	3.125 ns	20 ns	-7 V – 14 V
DG	RC clock	25 ns	20 ns	-7 V – 14 V
ϕR_{LH}	RC clock	3.125 ns	10 ns	-7 V – 14 V
$R\phi_{2HV}$	LC resonant clock	3.125 ns	Sinusoid at 10 MHz	-1.8 V – 61.8 V[1]
CLPIN	Digital (to ADC)	3.125 ns	–	–
Biases	DC	–	–	-5 V – 30 V[2]

[1] Software-limited to 50 V (configurable) to prevent exceeding the EMCCD absolute maximum rating.
[2] Depending on the bias. The range is adapted individually to the EMCCD typical range and absolute maximum rating.

that runs the image acquisition process. An external SRAM is used to hold the MicroBlaze program and data memory. The SRAM implements a Reed-Solomon IP core[14] to detect and correct errors of up to 4 bits per 16-bits words by using a parity of 16 bits. The Reed-Solomon automatically corrects errors on a read operation, but it is only during a write operation that the corrupted data is overwritten with the right one. For that reason, the whole SRAM is scrubbed periodically by a background task of the Microblaze to prevent the accumulation of uncorrected errors in parts of the memory that are seldom written or never written to by the E-SW.

5.4 Analog core

The CPE generates all of the required DC biases and clock signals to drive the EMCCD and synchronize the Analog to Digital Converter (ADC), as listed in Table 8. All clocks have low and high levels that are independently adjustable within the depicted range. The clock design accounted for the headboard length, for which its 15 cm transmission lines that have a significant effect at 10 MHz for the fast-edges.

All of the analog clocks are synchronized by a digital signal generated by the FPGA's sequencer. That signal dictates the state of the clock (low or high), and the analog part of the clock generation handles the shaping of the clock to the designed shape (triangular or RC), within the low and high levels set. The flexibility in the generation of the clocking schemes offered by the CPE design is of importance as this is what allows it to support, within the same hardware configuration, the different operational modes, from the 1 k fps imposed by the LOWFS mode to the 0.01 fps photon counting mode for the exoplanets imaging, that carry very different top level requirements (see Table 1).

5.5 Video signal sampling

The Electron Multiplying (EM) and CONV outputs of the EMCCD are sampled by Texas Instruments (TI) LM98640QML-SP ADC. The ADC is constantly running at 40 MSPS, which produces 4 samples per pixel at 10 MHz. Although the LM98640 has internal analog Correlated Double Sampling (CDS) capability, the ADC uses two sampling paths in that mode[15] and, during the TRL-5 project, they were found to produce a checkerboard pattern that could not be kept fixed from image to image. For that reason, it was decided to implement a DCDS within the FPGA to allow a reference sample to be subtracted from a signal sample. The DCDS implementation also allows the averaging of several reference or signal samples to reduce the effective noise. When reading-out the EMCCD through its CONV amplifier at 1 MHz, the 40 samples are processed in that way.

6. QUALIFICATION

6.1 Vibration campaign

The two CPEs flight models underwent random vibration testing at the CSA's David Florida Laboratory structural qualification facilities in Ottawa, Canada. Both units were tested at the qual vibration level of 10.3 gRMS in each axis. The enclosure units were tested with representative thermal strap and EMCCD headboard custom backshell dummy masses in order to fully represent the flight vibration loads. The two flight units were vibrated simultaneously (Figure 8).

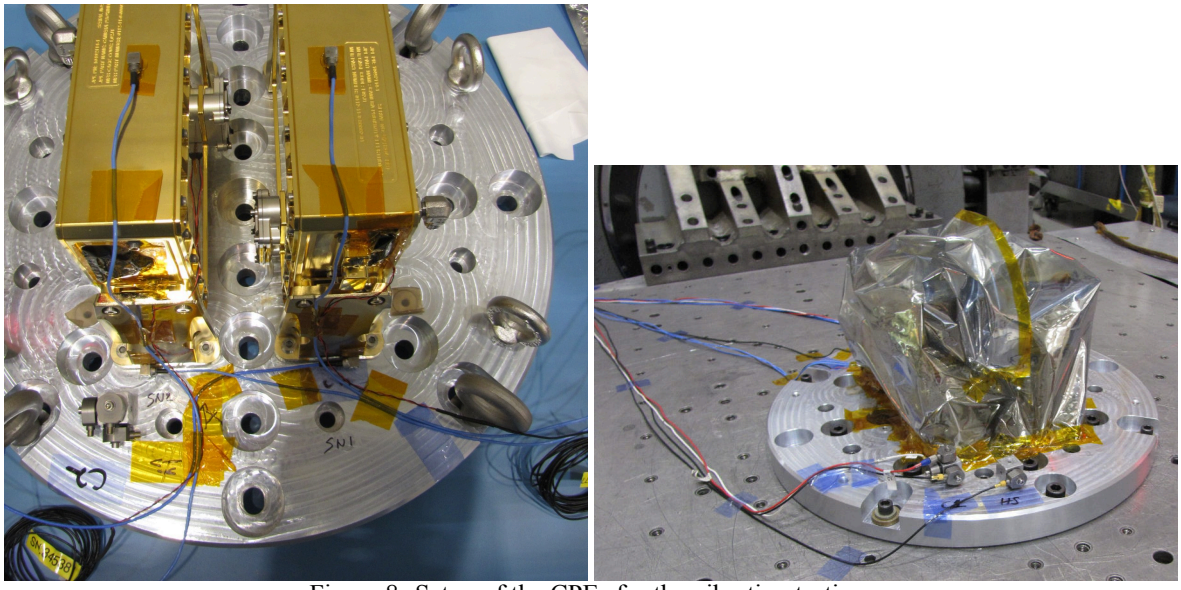

Figure 8: Setup of the CPEs for the vibration testing.

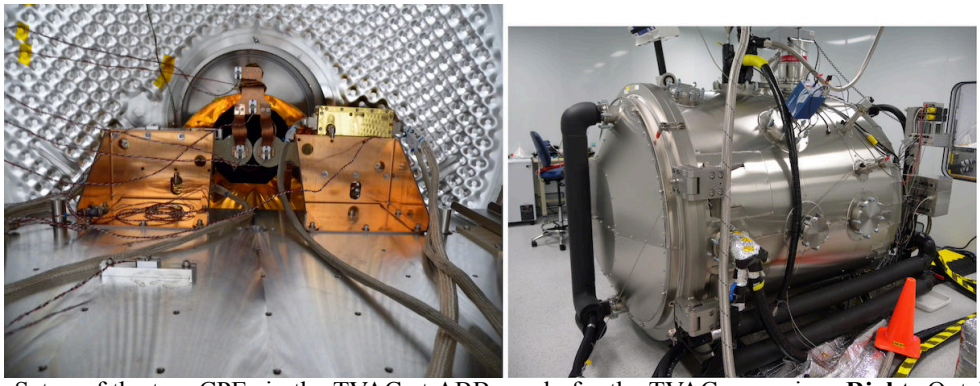

Figure 9: **Left**: Setup of the two CPEs in the TVAC at ABB, ready for the TVAC campaign. **Right**: Outside view of the TVAC in the clean room.

For all three vibration axes, low level signatures overlays did not show any significant differences for any of the accelerometers and structural modes did not shift by more than 5%. Final and between-axis visual inspections did not reveal any issue with both units. All post-vibration system bench tests were performed successfully.

6.2 Thermal vacuum campaign

6.2.1 Setup

The two CPEs flight models underwent Thermal Vacuum Chamber (TVAC) testing at ABB in Quebec City, Canada. Both CPE units were simultaneously tested with development program EMCCDs provided by JPL (Figure 9). The TVAC Optical Ground Support Equipment (OGSE) was designed to illuminate both EMCCDs with a flat field. Input light level was controlled with computerized motorized attenuators and feedback was monitored with a photodiode installed in an integration sphere. This allowed a repeatable input level for the multiple light fluxes required throughout the TVAC campaign.

EMCCDs were cooled down to -95°C with a CryoMech cooler while the CPE were cooled by controlling their thermal strap interface temperature with a circulating loop.

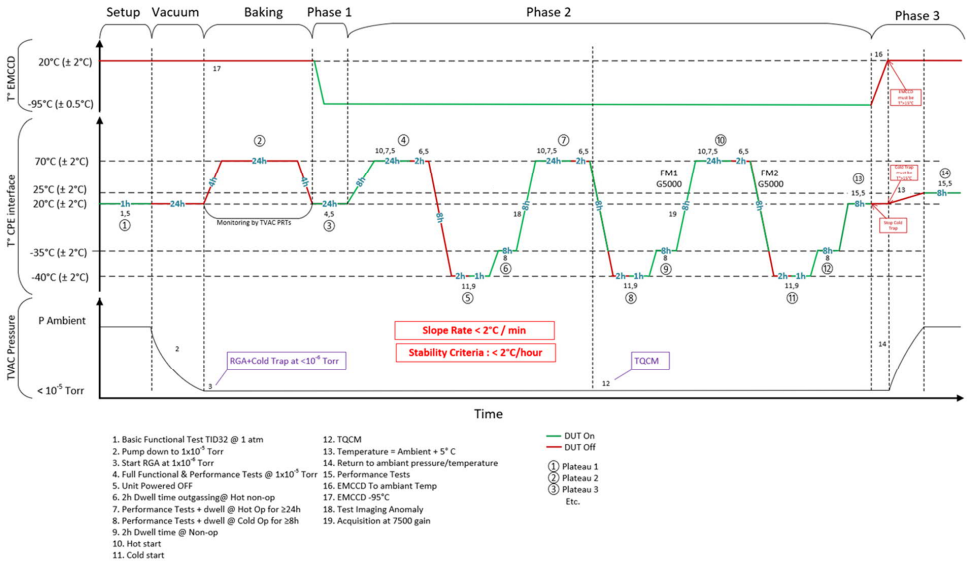

Figure 10: Pressure and temperature profiles for the TVAC campaign.

6.2.2 Thermal cycles

The CPEs underwent an initial outgassing cycle at +70°C. A total of 3 full thermal cycles were performed. In each thermal cycle, non-operational temperatures of -40°C and +70°C were reached, while CPE operation was demonstrated from -35°C to +70°C. After each non-operational plateau, an electronics start was performed. Electronics were operated at +70°C for a total of more than 72 hours (Figure 10).

A vacuum level lower than 10^{-6} torr was maintained throughout the TVAC campaign.

6.2.3 Performance evaluation

Full performance evaluation of the CPEs was performed throughout the TVAC campaign. Performance tests executed at each temperature plateau were the following:

- Basic Functional Test;
- EM Gain Stability;
- Charge Transfer Efficiency (CTE) through Extended Pixel Edge Response (EPER);
- EM Gain Characterization;
- Charge capacities;
- Power consumption;
- Photon transfer curve at unity gain;
- LOWFS Mode;
- Photon counting mode read noise.

Internal CPE thermal measurements showed that the thermal model was appropriate and slightly conservative. Post-TVAC inspections showed no issues and post-TVAC bench tests showed nominal performance.

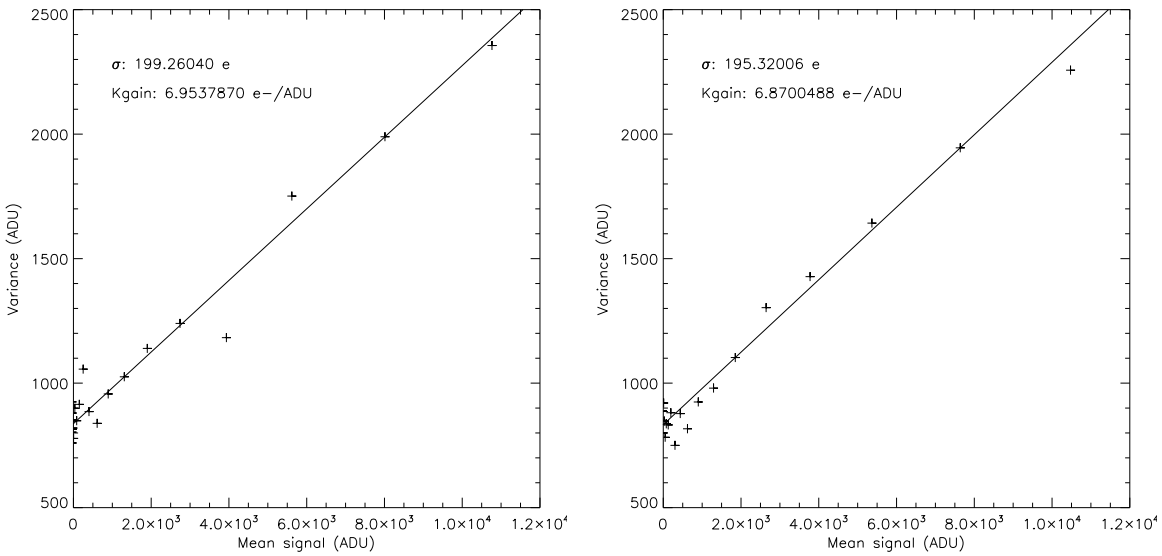

Figure 11: Photon Transfer Curve for both CPEs in TVAC. **Left**: SN1. **Right**: SN2.

7. PERFORMANCE RESULTS

The imaging performance of the flight CPEs was demonstrated at ABB in TVAC with a set-up similar to what is shown in Figure 6. The imaging performance tests were performed mostly at the hot plateaux (Figure 10), with basic functional tests performed at the cold excursions. The results are presented for both CPEs, arbitrarily named SN1 and SN2.

7.1 Read-out noise

The read-out noise of both CPEs was measured with the Photon Transfer Curve (PTC) method,[16] and by using increasing exposure time to generate a variation of the signal as seen by the EMCCD. The flight CPEs were first tested with a commercial CCD201-20 cooled in a Nüvü LN_2 dewar, that uses a commercial headboard. In that configuration, the CPEs achieved a read-out noise of $\sim$150 e^- by using a single sample for each of the reference and the signal level of the pixels for the DCDS processing. However, in the TVAC set-up where the performance had to be measured, noise coupling on the CGI FM headboards increased the noise level beyond the 200 e^- of the requirement. A second sample for the signal level had to be used and averaged to achieve the noise requirement. The resulting PTCs taken at 70°C for both CPEs are presented in Figure 11.

Post-devlivery tests at JPL revealed a ground loop generated by the headboard housing that caused the higher noise susceptibility. Noise figures akin to those obtained with the LN_2 dewar are now achieved.

7.2 EM gain stability

The EM gain stability was measured by taking images at a rate of one per second at the photon counting gain of $\sim$5000 and $\sim$7500 over 10 hours. During that time, the CPEs were reading-out a flight-equivalent EMCCD through the CGI headboards. The temperature of the EMCCDs was kept at -95°C by the TVAC set-up, and they were subjected to a stabilized faint light level of $\sim$0.1 photon/pix/s. The gain stability was then computed by measuring the mean signal level per image as seen in the detector. The high EM gain stability of the CPEs is presented in Figure 12. The disturbances in the gain level are expected to be caused by the EMCCD temperature that varied over the course of the acquisitions.

7.3 Charge Transfer Efficiency

The CTE at unity gain was measured with the EPER method.[16] The percentage of deferred charges measured in a row or a column after n transfers, P_{def}, can yield to the actual CTE of each transfer by means of the following equation:

$$CTE = \left(1 - P_{def}\right)^{1/n}. \quad (1)$$

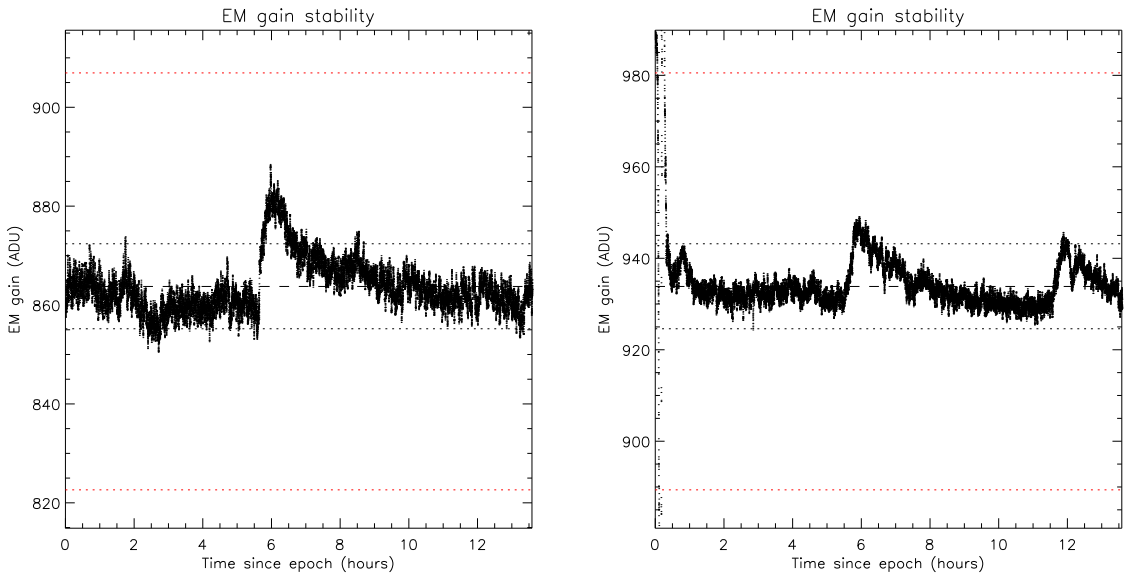

Figure 12: High gain stability. **Left**: SN1. **Right**: SN2. The red dotted lines represent a $\pm 5\%$ variation, and the black dotted lines a $\pm 1\%$ variation over the median.

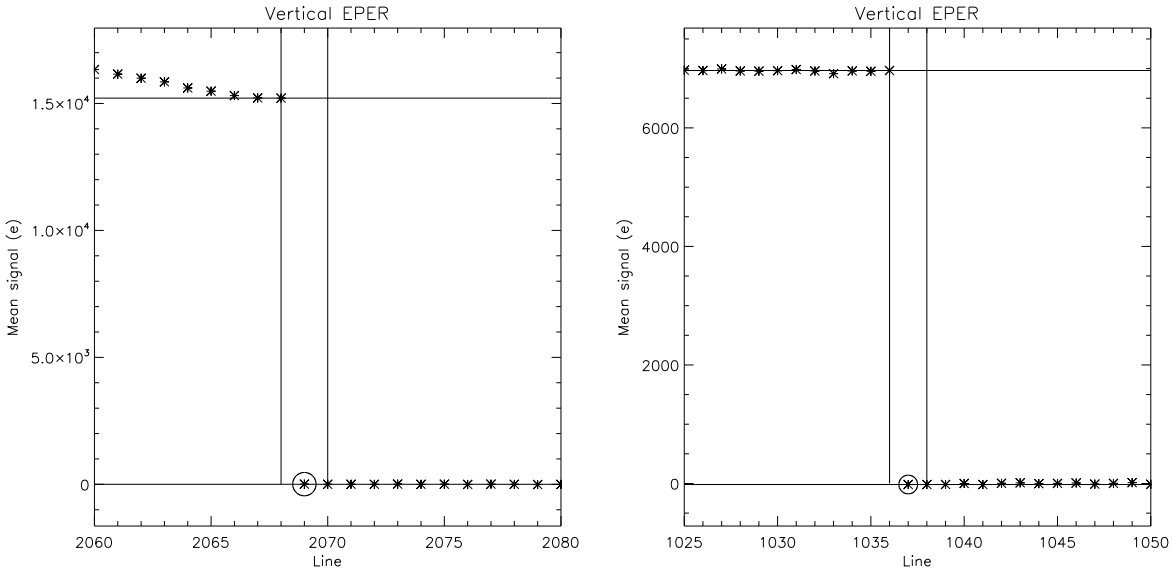

Figure 13: Vertical EPER graphs for CTE measurements. **Left**: SN1. **Right**: SN2.

Using that equation, the data in Figure 13 yields the value of 0.99999856 and 0.99999950 for the vertical CTE of both CPEs, respectively. The vertical lines denotes the signal and black levels, respectively, while the circled data point represents the pixel that contains the deferred charge. Differences in the illumination pattern on the EMCCD explain the dissimilarity of the data points shapes.

The unity gain horizontal CTE can be obtained in the same way, with the data presented in Figure 14. Those levels of deferred charges translate to a horizontal CTE of 0.99997050 an 0.99995986 for SN1 and SN2, respectively.

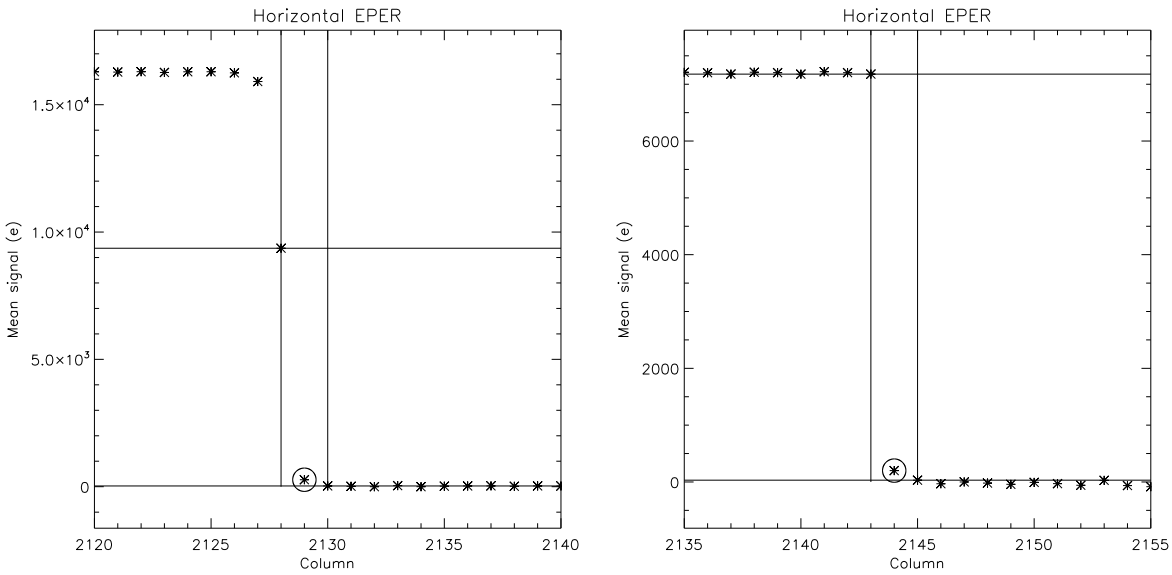

Figure 14: Horizontal EPER graphs for CTE measurements at unity gain. **Left**: SN1. **Right**: SN2.

7.4 CIC

The level of CIC generated by the new analog clocks design is slightly higher but comparable to what is usually seen with a commercial Nüvü controller when operating at a vertical frequency of 800 kHz and a horizontal frequency of 10 MHz for a given EM gain. Care must be taken when comparing those results with the litterature as the CIC is often reported for an EM gain of 1000. Results are presented in Figure 15 for SN1 and SN2. These numbers represent the results of the fit of the tail of the histogram, which gives at the same time the gain (slope) and the signal level (area under slope). This fit does not account for pixels that are counted due to the non-ideal CTE that makes the signal of a bright pixel leak into the following one, the so-called *bad pixels*.[17] When considering all of the pixels that have a signal level higher than 5σ, which represents what a simple Photon Counting thresholding algorithm would see as the signal level, the total background signal, which includes both the CIC and the dark current, is of $\sim$0.01e$^-$/pixel/frame in the image area at an EM gain of 7500 for a read-out size of 2000x2000 pixels.

7.5 LOWFS

The LOWFS mode required to read-out a small Region of Interest (ROI) of 50x50 pixels located on the edge of the EMCCD imaging area (Figure 16) at 1000 fps. A custom pipeline-compensation architecture had to be implemented in the FPGA to account for the mismatch between the width of the 50-pixels lines and the length of the EMCCD extended horizontal register, whilst providing the capability to adjust the position of the ROI by up to (10,10) pixels (Figure 17) and keep the latency minimal.

The LOWFS mode prevents the accumulation of the light in the ROI by back-clocking the Image and Store sections after the completion of the read-out. This back-clocking is made before emptying the EMCCD pipeline, which consists of 17 full lines of the ROI. That way, the exposure of the next frame effectively starts during the reading of the pipeline. This allows the worst-case effective exposure time per frame to be $\sim$475μs (with a (10,10) offset) for a total read-out time of $\sim$635μs at 1000 fps, and meets the $<$1 ms latency requirement.

The back-clocking causes a slight disturbance on the video signal, which appear as a brighter line in the LOWFS images (Figure 17). That structure is static and does not impair the LOWFS algorithm as it is differential.[19]

8. CONCLUSIONS

From the early EMCCD maturing activities undertaken at JPL, the work continued to develop the the full camera system, including the read-out electronics. This paper presented the mechanical, thermal, and electronic designs of the NGRST

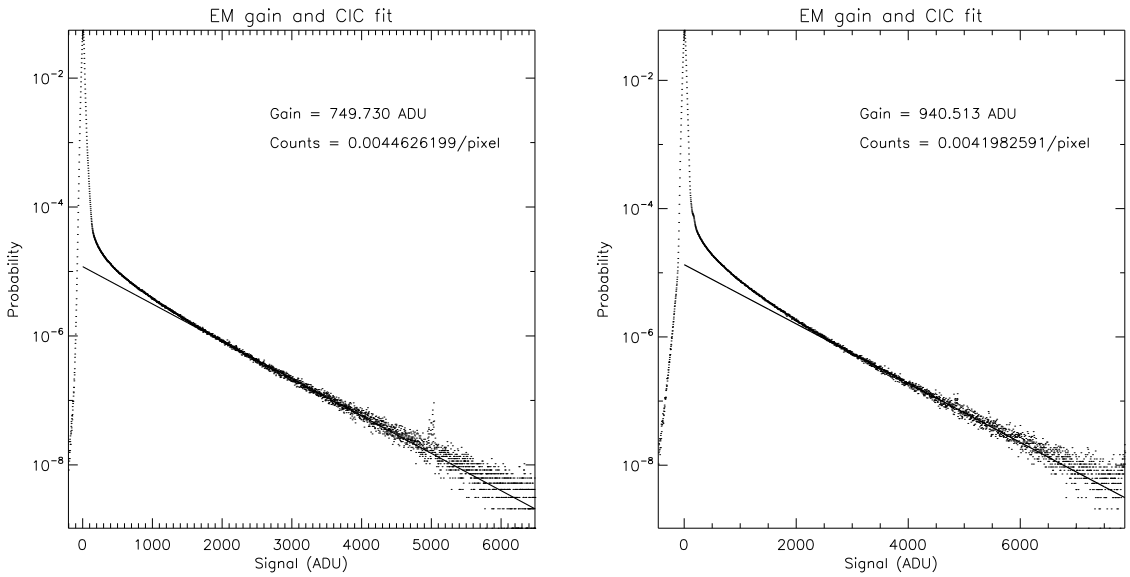

Figure 15: Background signal level (mainly CIC) level of 0-s integration frames. **Left**: SN1 at gain ∼5000. **Right**: SN2 at gain ∼7500.

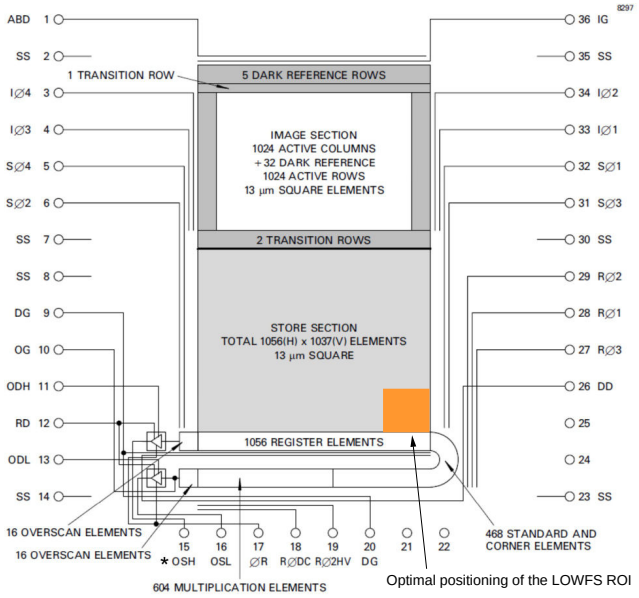

Figure 16: Position of the LOWFS ROI with respect to the CCD201-20 architecture (image adapted from [18]). For the CCD301, the store shield is not present.

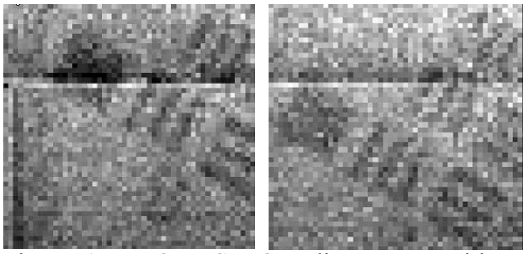

Figure 17: LOWFS ROI adjustment positioning adjustment, showing the capability to move by (10,10) pixels on a subsection of a standard USAF target, under low light and moderate gain.

CGI EMCCD flight camera electronics, as well as some of the performance data that were acquired during the qualification campaign for the two flight CPEs that were delivered to JPL. The designs has passed JPL's SMA requirements, were shown to meet the performance requirement in TVAC, and passed vibration testing. The two flight modules are now being further integrated at JPL into the CGI as the LoCam and ExCam CPEs.

Building on the design of the Roman CGI CPEs, Nüvü Camēras is now developing an EMCCD solution for small satellites and cube sats.

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